Silicon IQ Modulator for 120 Gbaud QAM

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Abstract *We experimentally demonstrate an all-silicon IQ modulator with a segmented design operating at 120 Gbaud 32QAM. We achieve BER below the 25% FEC-threshold for a line-rate of 600 Gb/s (net 480 Gb/s) on a single polarization.*

Introduction

Segmented modulators are particularly well adapted to higher order modulation[1]. In silicon photonic (SiP) modulator design, a shorter phase shifter has better bandwidth, but larger V_π. This results in a classic trade-off involving many subtleties in overall system bit error rate (BER) performance optimization[2]. Dividing one phase shifter in two equal lengths improves the bandwidth as each drive signal sees a shorter electrode. However, the overall phase shift (determined by the total phase shifter length) is the same whether as a single segment or divided into two equal segments. In contrast, segmented modulators designed for operation without a digital to analog converter (DAC), a phase shifter is divided into unequal lengths to achieve multiple level signals from binary drive signals. In this design, both bandwidth and V_π are different for each segment. We examine how performance can be improved when driving the unequal segments, not with independent binary signals, but rather with identical multilevel data streams.

In[3] our single segment 4.5 mm phase shifter achieved 32QAM 100 Gbaud with BER below 2e-2. That modulator had 3 dB bandwidth of $\sim$35 GHz with V_π around 6.5V. In this paper we use segmentation to improve the MZM bandwidth (up to 63 GHz) while lowering V_π to push the baud rate to 120 Gbaud. In[4], 120 Gbaud with a SiP modulator was limited to QPSK. In our single polarization demonstration, we achieve 120 Gbaud 16QAM at BER 6.4e-3, and 120 Gbaud 32QAM at BER 3.8e-2. To best of our knowledge, this is the first demonstration of 120 Gbaud high order QAM generation using an all silicon modulator.

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Device Design and Characterization

The schematic of our device is shown in Fig. 1. It consists of two Mach-Zehnder modulators (MZM) for IQ operation, each having four different-length segments of phase shifters applying traveling-wave (TW) electrodes. This segmented design allows us to increase the overall phase shifter without scarifying the bandwidth and thus is effective to lower the drive voltage, but requires an RF chain for each segment driver. Only the two longest segments (2 and 4 mm) were used in our experiment. Laterally doped p-n junctions in 220-nm-high silicon rib waveguides are used as the phase shifters, where three levels of dopants are applied to reduce the junction resistance without introducing excess optical loss. The MZM uses a series push-pull driving configuration, which imposes lower capacitive load for a higher bandwidth. Each TW-phase shifter uses a coplanar stripline transmission line with on-chip 50Ω termination implemented using semiconductor resistors. More details of the TW phase-shifter design can be found in[2]. The phase shifters are characterized by a $V_\pi L$ of about 3V-cm for a large voltage swing. A thermally tunable 2$\times$2 Mach-Zehnder interferometer is used at input of each MZM, allowing us to maximize the optical extinction ratio and to test the I and Q branches separately. The MZM has an optical loss of $\sim$21.5 dB, including $\sim$12 dB due to fiber-to-chip coupling and $\sim$3 dB due to long waveguide routing (not shown in Fig. 1).

We measured the S21 of one branch of the IQ modulator at various bias voltages with a 67 GHz vector network analyser (VNA). The S21 for the long (4 mm) and short (2 mm) segments are given in Fig. 2a and 2b, respectively, for various bias voltages. We measure PAM4 symbol error rate

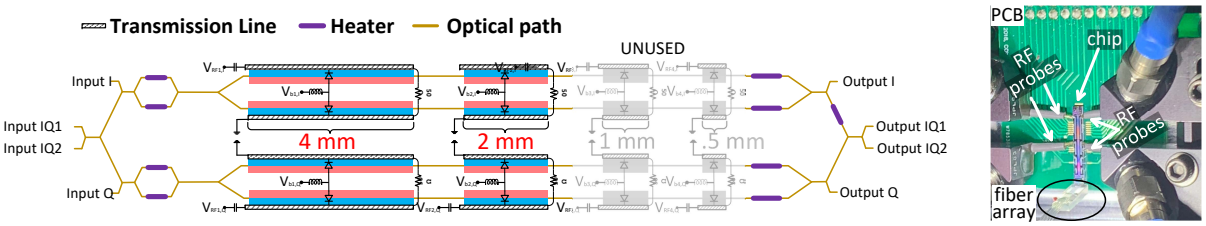
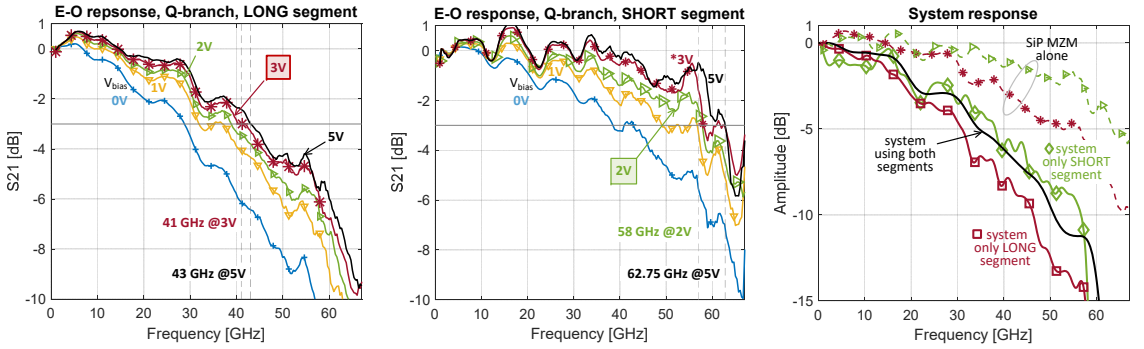


Fig. 1: Schematic of the chip design (left) and photo of chip under test (right).



(a) (b) (c)

Fig. 2: Frequency response of a) LONG MZM segment, b) SHORT MZM segment, c) overall system response when using each segment independently and when sending identical data streams to each segment simultaneously

(SER) at 120 Gbaud while sweeping bias voltage at half volt intervals. Optimal SER occurred at 3V and 2V bias for the long and short segments, respectively. At these optimal bias voltages, the 3 dB bandwidth was 41 GHz for the long segment, and 58 GHz for the short segment. Note that while bandwidth is greater at 5V bias (near 63 GHz for the short segment), this choice limits the V_π and overall SER performance degrades. We use coherent reception to estimate the tandem drive system frequency response, as the VNA cannot handle both segments in tandem.

As we target aggressive baud rates that exceed the transmitter bandwidth, DACs are unavoidable. Pulse shaping and pre-equalization curtails the available drive voltage. For our equipment at 120 Gbaud, the peak-to-peak swing was $V_{pp} = 4$V. We transmit 120 Gbaud PAM4 with raised cosine filtering with rolloff of .01 and digital pre-compensation for DAC frequency response. We estimate three response (long segment alone, short segment alone, tandem). The drive signals are identical in all three cases. In Fig. 2c we replot the VNA MZM S21 measurement at the optimal bias in dashed lines; solid lines show the overall system response including effects from the RF chain (phase shifters used to synchronize timing, RF amplifiers, DAC and modulator segments), as well as from the real time oscilloscope and photodiodes for coherent detection. Lines with markers show the bandwidth is reduced significantly for the system vis-à-vis the MZM. The tandem system response is given by the solid line without markers. It most closely tracks the contribution from the wider band, shorter segment. Were the system linear, the concatenation of two frequency responses filtering identical drive signals would have an effective frequency response that is the sum of the two responses. The sum would then be dominated by the wider band response. Although the system is not linear, we are able to retain the wider bandwidth of the shorter segment, while enjoying the phase displacement enabled by the total length of two phase shifters.

Transmission Experiment and Results

The experimental setup is shown in Fig. 3. An external cavity laser (ECL) at 1550 nm with 100 kHz linewidth is boosted to 28 dBm by a high power erbium doped fiber amplifier (EDFA). We couple to the silicon chip via a fiber array and operate at the null point, probing I and Q drive signals for each segment L (long) and S (short). While data sequences are identical, separate DAC channels are used to individually pre-equalize each segment frequency response. Data is prepared offline per the digital signal processing (DSP) flowchart in Fig. 3. Random data is mapped to Grey-coded (16 or 32) QAM symbols, then shaped to raised-cosine with roll-off factor of 0.01. We pre-equalize by minimizing mean square error for the RF chain to each segment, as well

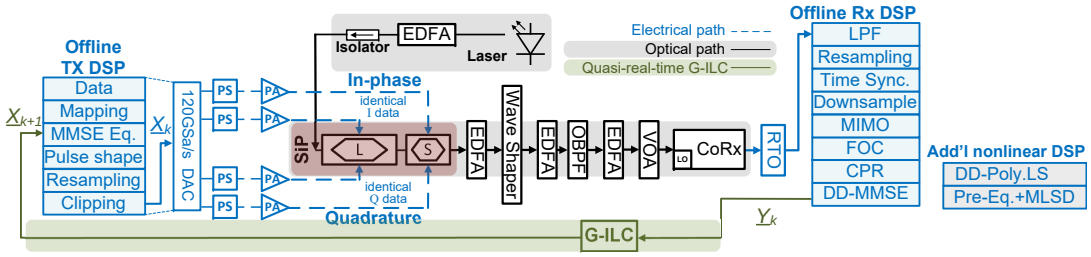


Fig. 3: Block diagram of DSP and experimental set-up

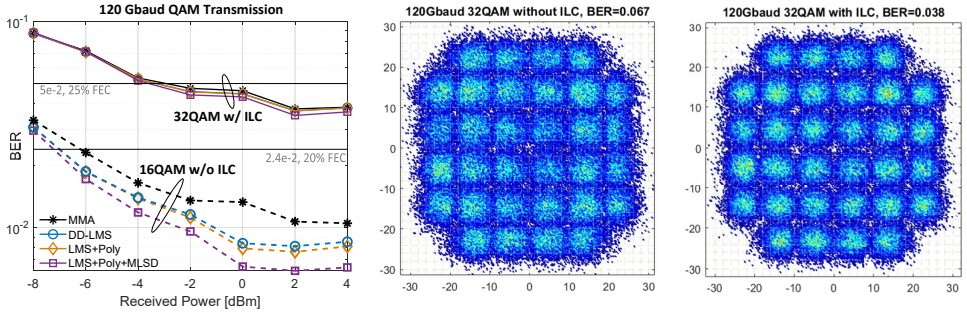


Fig. 4: Right, BER results for 16QAM and 32QAM; left,32QAM constellations before and after ILC pre-compensation.

as the receiver. Note that data is identical to each branch, but signals are different due to pre-equalization tailored to each segment. We operate a Micram VEGA5 8 bit DAC at one sample per symbol at 120 Gbaud using clipping and quantization. We compensate RF path delays via the RF phase shifters (PS) and amplify with 60 GHz 16 dBm (SHF S804B) RF drivers.

At the receiver side, DSP includes a 10^{th} order super Gaussian digital filter, resampling, T/4 spaced 2×2 multi-modulus algorithm (MIMO). We downsample to one one sample per symbol for frequency offset compensation (FOC), carrier phase recovery (CPR) by blind phase search, and a decision-directed minimum mean square error (DD-MMSE) equalizer. To enhance post-compensation we cascade a decision-directed memory polynomial least square (DD-Poly-LS) filter with 1^{st} and 3^{rd} order terms, and partial response equalization via a one-tap maximum likelihood sequence detector (MLSD). Finally, to improve bit error rate (BER), we employ nonlinear predistortion based on the iterative learning control (ILC) technique described in detail in[3]. The green shaded path in Fig. 3 shows the quasi-real-time adaptation with hardware-in-the-loop.

We use a two-stage EDFA at the chip output to compensate for optical insertion losses. An optical filter (Finisar Waveshaper) provides additional pre-equalization; the digital and optical pre-equalization were jointly optimized[5]. Two optical bandpass filters (OBPF) suppress out-of-band amplified spontaneous emission noise. We sweep received optical power with a variable optical attenuator (VOA). We use a discrete coherent receiver (CoRx) with 70 GHz bandwidth and a local oscillator (LO) with 15 dBm power. We capture electrical signals with a Keysight 160 GSa/s, 63 GHz, real-time oscilloscope (RTO) .

Figure 4 gives BER results following each of the final four steps in the DSP post-processing. For 16QAM we do not need the ILC pre-processing to reach the 20% FEC threshold; additional nonlinear post-processing provides greater margin. For 32QAM, ILC provides appreciable improvement, as seen in the constellations presented to the left in Fig. 4. The linear post-processing is sufficient for the 32QAM performance to fall under the 25% FEC threshold at 5e-2 BER.

Conclusions

We have achieved 16QAM and 32QAM back-to-back transmissions at 120 Gbaud with a segmented SiP IQ modulator for up to 480 Gb/s net rate per single polarisation when accounting for a 25% overhead FEC. To the best of our knowledge, this is the first demonstration of 120 Gbaud higher-order QAM operation using an all-silicon modulator.

Acknowledgements

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